	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
3	BRS	L3	88	digit same lines and imbalance and column and semiconductor	USPAT; US-PGPUB	2003/11/17 09:29			0
4	BRS	L4	3	digit same lines and imbalance and column and semiconductor and serpentine	USPAT; US-PGPUB	2003/11/17 09:31			0

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
47	BRS	38742	metallization and layer	USPAT; US-PGPUB; DERWENT	2003/11/12 15:27		
48	BRS	440	metallization and layer and semiconductor and serpentine	USPAT; US-PGPUB; DERWENT	2003/11/12 15:27		
49	BRS	300	metallization and layer same semiconductor and serpentine	USPAT; US-PGPUB; DERWENT	2003/11/12 15:27		
50	BRS	98	metallization same layer same semiconductor and serpentine	USPAT; US-PGPUB; DERWENT	2003/11/12 15:37		
51	BRS	42	metallization same layer same semiconductor and serpentine and memory	USPAT; US-PGPUB; DERWENT	2003/11/12 15:29		
52	BRS	4	metallization same layer same semiconductor and serpentine and (RAM or ROM)	USPAT; US-PGPUB; DERWENT	2003/11/12 15:30		
53	BRS	24	metallization same layer same semiconductor and orthogonal and ROM	USPAT; US-PGPUB; DERWENT	2003/11/12 15:56		
54	BRS	20643	metalization and pattern	USPAT; US-PGPUB; DERWENT	2003/11/12 15:56		
55	BRS	14886	metalization and pattern and semiconductor	USPAT; US-PGPUB; DERWENT	2003/11/12 15:56		
56	BRS	261	metalization and pattern and semiconductor and column same select	USPAT; US-PGPUB; DERWENT	2003/11/12 15:57		
57	BRS	66	metalization and pattern and semiconductor and column same select and orthogonal	USPAT; US-PGPUB; DERWENT	2003/11/12 15:57		

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Inventor Name Search Result

Your Search was:

Last Name = THOMPSON
First Name = J. WAYNE

Application#	Patent#	Status	Date Filed	Title	Inventor Name 4
10309572	Not Issued	030	12/03/2002	APPARATUS AND METHOD FOR A CURRENT LIMITING BLEEDER DEVICE SHARED BY COLUMNS OF DIFFERENT MEMORY ARRAYS	THOMPSON, J. WAYNE
09805913	Not Issued	095	03/15/2001	IMPROVED METAL WIRING PATTERN FOR MEMORY DEVICES	THOMPSON, J. WAYNE
08848529	5751031	150	04/28/1997	MEMORY AND OTHER INTEGRATED CIRCUITRY HAVING A CONDUCTIVE INTERCONNECT LINE PITCH OF LESS THAN 0.6 MICRON	THOMPSON , J. WAYNE
08431900	Not Issued	166	05/01/1995	MEMORY AND OTHER INTEGRATED CIRCUITRY HAVING ELECTRICALLY CONDUCTIVE INTERCONNECTS	THOMPSON , J. WAYNE

Inventor Search Completed: No Records to Display.

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Last Name	First Name
thompson	j. wayne

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Inventor Name Search Result

Your Search was:

Last Name = MERRITT
First Name = TODD

Application#	Patent#	Status	Date Filed	Title	Inventor Name 51
10338565	6654306	150	01/07/2003	APPARATUS AND METHOD FOR GENERATING AN OSCILLATING SIGNAL	MERRITT, TODD A.
10338191	Not Issued	082	01/07/2003	VOLTAGE PUMP AND A LEVEL TRANSLATOR CIRCUIT	MERRITT, TODD A.
10326887	Not Issued	019	12/20/2002	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
10317847	Not Issued	019	12/11/2002	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
10293789	Not Issued	030	11/12/2002	METHOD AND STRUCTURES FOR REDUCED PARASITIC CAPACITANCE IN INTEGRATED CIRCUIT METALLIZATONS	MERRITT, TODD A.
10232978	Not Issued	092	08/29/2002	DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES	MERRITT, TODD A.
10232977	Not Issued	041	08/29/2002	DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES	MERRITT, TODD A.
10232092	Not Issued	041	08/29/2002	DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES	MERRITT, TODD A.
10231942	Not Issued	071	08/29/2002	DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES	MERRITT, TODD A.
10231682	Not Issued	093	08/29/2002	DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES	MERRITT, TODD A.
10029572	RE38109	150	12/20/2001	BLOCK WRITE CIRCUIT AND METHOD FOR WIDE DATA	MERRITT, TODD A.

				CHARGE PUMP	
09790425	6407939	150	02/21/2001	SINGLE DEPOSITION LAYER METAL DYNAMIC RANDOM ACCESS MEMORY	MERRITT, TODD A.
09773676	6363032	150	02/02/2001	PROGRAMMABLE COUNTER CIRCUIT FOR GENERATING A SEQUENTIAL/INTERLEAVE ADDRESS SEQUENCE	MERRITT, TODD A.
09747352	6560728	150	12/19/2000	LAYOUT FOR A SEMICONDUCTOR MEMORY DEVICE HAVING REDUNDANT ELEMENTS	MERRITT, TODD A.
09741368	6307398	150	12/19/2000	LOW POWER, HIGH SPEED LEVEL SHIFTER	MERRITT, TODD A.
09711405	Not Issued	161	11/13/2000	MEMORY DEVICE WITH BLOCK WRITE BURST.	MERRITT, TODD A.
09659247	6452845	150	09/11/2000	APPARATUS FOR TESTING REDUNDANT ELEMENTS IN A PACKAGED SEMICONDUCTOR MEMORY DEVICE	MERRITT, TODD A
09652996	6327167	150	08/31/2000	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
09652839	6320779	150	08/31/2000	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
09652587	6314012	150	08/31/2000	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
09652586	6301142	150	08/31/2000	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
09652584	6438011	150	08/31/2000	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
09652578	6301141	150	08/31/2000	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
09652390	Not Issued	093	08/31/2000	SYSTEM AND METHOD FOR IMPLEMENTING DATA PRE-FETCH HAVING REDUCED	MERRITT, TODD A.

				DATA LINES AND/OR HIGHER DATA RATES (AS AMENDED)	
09651332	6259270	150	08/31/2000	SEMICONDUCTOR PROGRAMMABLE TEST ARRANGEMENT SUCH AS AN ANTIFUSE ID CIRCUIT HAVING COMMON PROGRAMMING SWITCHES	MERRITT, TODD A.
09645577	6333882	150	08/25/2000	EQUILIBRATION/PRE-CHARGE CIRCUIT FOR A MEMORY DEVICE	MERRITT, TODD A.
09644940	6356487	150	08/23/2000	MEMORY DEVICE HAVING DATA PATH CONTAINING DUAL MODE FLIP-FLOP USED FOR NORMAL OPERATION AND FOR INTERNAL TESTING	MERRITT, TODD A.
09609935	6215729	150	06/30/2000	PROGRAMMABLE COUNTER CIRCUIT FOR GENERATING A SEQUENTIAL/INTERLEAVE ADDRESS SEQUENCE	MERRITT, TODD A.
09573074	6484278	150	05/16/2000	METHOD AND APPARATUS FOR TESTING AN EMBEDDED DRAM	MERRITT, TODD A.
09560121	Not Issued	041	04/28/2000	HIGH OUTPUT HIGH EFFICIENCY LOW VOLTAGE CHARGE PUMP	MERRITT, TODD A.
09544560	6205078	150	04/06/2000	METHOD AND APPARATUS FOR TRANSLATING SIGNALS	MERRITT, TODD A.
09531023	6365421	150	03/20/2000	METHOD AND APPARATUS FOR STORAGE OF TEST RESULTS WITHIN AN INTEGRATED CIRCUIT	MERRITT, TODD A.
09511577	6285243	150	02/23/2000	HIGH-VOLTAGE CHARGE PUMP CIRCUIT	MERRITT, TODD A.
09510021	6351421	150	02/22/2000	IMPROVED DATA OUTPUT BUFFER	MERRITT, TODD
09492412	6353549	150	01/27/2000	ARCHITECTURE AND PACKAGE ORIENTATION FOR HIGH SPEED MEMORY DEVICES	MERRITT, TODD A.
09490803	6205085	150	01/26/2000	METHOD AND CIRCUIT FOR SENDING A SIGNAL IN A SEMICONDUCTOR DEVICE DURING A SETUP TIME	MERRITT, TODD A
09482912	6166942	150	01/14/2000	EMBEDDED DRAM ARCHITECTURE WITH LOCAL DATA DRIVERS AND PROGRAMMABLE NUMBER OF	MERRITT, TODD A.

DATA READ AND DATA WRITE LINES

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Last Name	First Name
merritt	todd

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Results 1 - 3 of 3 short listing

1 Automatic circuit analysis based on mask information 77%
B. T. Preas , B. W. Lindsay , C. W. Gwyn
The proceedings of the thirteenth design automation conference on Design automation June 1976
A Circuit MAsk Translator (CMAT) code has been developed which converts integrated circuit mask information into a circuit schematic. Logical operations, pattern recognition, and special functions are used to identify and interconnect diodes, transistors, capacitors, and resistances. The circuit topology provided by the translator is compatible with the input required for a circuit analysis program.

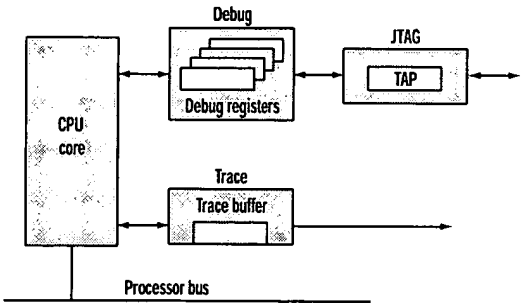
2 CAD for military systems, an essential link to LSI, VLSI and VHSIC technology 77%
Randolph Reitmeyer
Proceedings of the eighteenth design automation conference on Design automation June 1981
Government involvement in the development of computer aided design (CAD) tools for electronic circuits has a long history. The advent of large scale integrated (LSI) circuits, going into the 1970's, pulsed the development of the “standard cell” and “gate array” design methodologies and supporting CAD. Despite these burgeoning technologies, little custom LSI technology found its way into military systems. Custom LSI was considered too costly and risky.

3 Accurate interconnect modeling: towards multi-million transistor chips as microwave circuits 77%
N. P. van der Meijs , T. Smedes
Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997
In this tutorial we discuss concepts and techniques for the accurate and efficient modeling and extraction of interconnect parasitics in VLSI designs. Due to increasing operating frequencies, microwave-like effects will become important. Therefore stronger demands are put on extraction and verification tools. We indicate the state-of-the-art for capacitance, resistance and

				PATH MEMORY DEVICES	
10017517	6501669	150	12/11/2001	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
10017515	6545894	150	12/11/2001	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
10007571	6504743	150	11/07/2001	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
10006785	Not Issued	140	11/09/2001	OUTPUT BUFFER HAVING INHERENTLY PRECISE DATA MASKING	MERRITT, TODD A.
10005087	6498740	150	12/04/2001	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
09999094	Not Issued	164	10/30/2001	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
09964134	6430075	150	09/25/2001	DIE ARCHITECTURE ACCOMMODATING HIGH-SPEED SEMICONDUCTOR DEVICES	MERRITT, TODD A.
09945511	6578165	150	08/30/2001	INTERNAL GUARDBAND FOR SEMICONDUCTOR TESTING	MERRITT, TODD A.
09945253	6577552	150	08/30/2001	APPARATUS AND METHOD FOR GENERATING AN OSCILLATING SIGNAL	MERRITT, TODD A.
09938646	6556643	150	08/27/2001	MAJORITY FILTER COUNTER CIRCUIT	MERRITT, TODD
09927373	6490220	150	08/13/2001	METHOD FOR RELIABLY SHUTTING OFF OSCILLATOR PULSES TO A CHARGE-PUMP	MERRITT, TODD A.
09922982	6384669	150	08/06/2001	HIGH VOLTAGE CHARGE PUMP CIRCUIT	MERRITT, TODD A.
09873463	6385709	150	06/04/2001	MULTIPLEXED DATA TRANSFER ARRANGEMENT INCLUDING A MULTI-PHASE SIGNAL GENERATOR FOR LATENCY CONTROL	MERRITT, TODD A.
09797320	Not Issued	041	03/01/2001	HIGH OUTPUT HIGH EFFICIENCY LOW VOLTAGE	MERRITT, TODD A.

On-Chip Debugging Series

and must be restarted via a reset. There also is a 48-bit clock cycle counter, the RUNN counter, for precise cycle control. It can be set to a count and counts down to zero, where it stops the clocks. It can be triggered by a number of signals and events, including interrupts.



Motorola added a Service bus to debug. Instead of scan chains to access key latches, they're directly addressable via Service Access. Up to 16 bits can be set or reset at the same time for a single Service Register Access. These registers are accessed via a Service Access JTAG command.

IBM has built on the PowerPC base, fielding PPC cores and PPC ASSPs. The cores include the 405 RISC, and the ASSPs include communications engines like the 440 GP, a 32-bit RISC SoC that integrates a 32-bit PPC core with a PCI-X bridge, a DDRAM controller, and a DMA controller. These PPCs incorporate an extension of the Book-E design. Instead of a single Debug Mode, they define four modes:

- Internal Debug Mode—supports ROM monitors.
- External Debug Mode—supports JTAG debuggers (Book-E Internal Debug Mode).
- Debug Wait Mode—supports CPU stop/stepping for JTAG while servicing interrupts.
- Real-Time Trace Mode—supports trigger events for real-time trace.

Debug events trigger a debug operation, which depends on the current Debug Mode. Internal Debug Mode supports setting and reacting to hardware and software breakpoints. The debug events can interrupt normal program flow for a debug monitor, while the programs continue to run.

One debug control is to "Freeze Timers." This can be triggered by the JTAG debug port, or via a bit set in the Debug Control Register 0. Timers can be enabled to run, freeze always, or freeze on a debug event. Freeze enables the code to ignore the time in debug, keeping a semblance of real-time count.

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